IN THE CLAIMS

Please amend the claims as follows:

Claims 1 and 2 (Canceled).

3. (Currently Amended): ~~The~~ A microprocessor ~~as claimed in claim 2, wherein the memory management unit comprises:~~ comprising:

a processor core including an instruction executing unit configured to execute instructions for input and output controlling and processing for data and a cache memory configured to store the data;

a memory management unit coupled to the processor core, the memory management unit configured to manage memory system including the cache memory, the memory management unit comprising

a pre-routing storing unit configured to store [[the]] pre-routing information that indicates the connection state of signals of [[the]] a switching circuit[[;]], and

an address translation buffer configured to store virtual tag information for translating virtual addresses generated inside the processor into physical addresses, each of the virtual tag information is stored by an entry and corresponds to bus switch control information for controlling a connection relationship of a bus switch; and

a bus interface coupled to the processor core and the memory management unit, the bus interface configured to rearrange an order of bits of the data transferred from the processor core, the bus interface comprising

a data input/output unit coupled to the processor core and memory management unit, the data input/output unit configured to receive and send the data,

the switching circuit coupled to the data input/output unit, the switching circuit configured to receive the data to change the order of the bits of the data according to the pre-routing information, and

the bus switch coupled to the switching circuit and configured to receive the data and change the order of the bits per a predetermined number of the bits according to the bus switch control information corresponding to an entry in the address translation buffer.

4. (Original): The microprocessor as claimed in claim 3, wherein the switching circuit changes connection state of signals according to the pre-routing information to change the order of bits.

5. (Original): The microprocessor as claimed in claim 4, wherein the pre-routing information is transferred from the memory management unit to the switching circuit when the data is to be outputted to a destination outside the processor.

6. (Original): The microprocessor as claimed in claim 2, wherein the switching circuit changes the order of bits of the data per a bit.

7. (Original): The microprocessor as claimed in claim 3, wherein the bus switch changes connection state of signals based on bus switch control information to change the order of bits of the data.

8. (Original): The microprocessor as claimed in claim 7, wherein the bus switch control information is stored by the memory management unit.

9. (Currently Amended): The microprocessor as claimed in claim [[2]] 3, wherein the bus switch changes the order of bits per a page managed by the memory management unit.

10. (Original): The microprocessor as claimed in claim 7, wherein the memory management unit stores the bus switch control information in each entry of the address translation cache memory.

11. (Original): The microprocessor as claimed in claim 7, wherein the bus switch control information is stored by an entry of the cache memory in the processor core.

12. (Original): The microprocessor as claimed in claim 9, wherein the bus switch receives the bus switch control information when an external address is accessed by the processor then the bus switch changes the order of bits of the data based on the bus switch control information.

13. (Currently Amended): The microprocessor as claimed in claim [[20]] 3, wherein the memory management unit includes a bus switch control information storing unit storing the bus switch control information, the memory management unit transfers the bus switch control information corresponding to a physical address stored in the address transfer cache memory when an external address is accessed by the processor.

Claims 14 and 15 (Canceled).

16. (Currently Amended): ~~The~~ A video/sound processing system ~~as claimed in claim 15, wherein the memory management unit comprises:~~ comprising:

a storage device configured to store content;

a bridge coupled to the storage device, the bridge configured to transfer the content stored by the storage device;

a microprocessor including

a processor core including an instruction executing unit configured to execute instructions for input and output controlling and processing for data and a cache memory configured to store the data

a memory management unit coupled to the processor core, the memory management unit configured to manage a memory system including the cache memory, the memory management unit comprising

a pre-routing storing unit configured to store [[the]] pre-routing information that indicates the connection state of signals of [[the]] a switching circuit[[;]], and

an address translation buffer configured to store virtual tag information for translating virtual addresses generated inside the processor into physical addresses, each of the virtual tag information is stored by an entry and corresponds to bus switch control information for controlling a connection relationship of a bus switch, and

a bus interface coupled to the processor core and the memory management unit, the bus interface configured to rearrange bits of the data transferred from the processor core, the bus interface comprising

a data input/output unit coupled to the processor core and memory management unit, the data input/output unit configured to receive and send the data,

the switching circuit coupled to the data input/output unit, the switching circuit configured to receive the data to change an order of the bits of the data according to the pre-routing information, and

the bus switch coupled to the switching circuit and configured to receive the data and change the order of the bits per a predetermined number of the bits according to the bus switch control information corresponding to an entry in the address translation buffer;

a memory coupled to the bridge, the memory configured to temporarily hold the rearranged content from the microprocessor; and

a D/A converter coupled to the memory, the D/A converter configured to convert the transferred content to analog data.

17. (Original): The video/sound processing system as claimed in claim 16, wherein the switching circuit changes connection state of signals according to the pre-routing information to change the order of bits of the content.

18. (Original): The video/sound processing system as claimed in claim 17, the pre-routing information is transferred from the memory management unit to the switching circuit when the content is to be outputted to a destination outside the processor.

19. (Currently Amended): The video/sound processing system as claimed in claim [[15]] 16, wherein the switching circuit changes the order of bits of the content per a bit.

20. (Original): The video/sound processing system as claimed in claim 16, wherein the bus switch changes connection state of signals based on bus switch control information to change the order of bits of the content.